Anh Tran

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EDUCATION

University of Pennsylvania, M.S.E. in Electrical Engineering – GPA: 3.93/4.0 Sep 2024 – May 2026
Relevant coursework: System-on-a-Chip Architecture, Hardware Security, Computer Organization & Design, General-Purpose GPU Architecture, HW–SW Co-Design for ML, Digital IC & VLSI Fundamentals

VinUniversity, B.Sc in Electrical Engineering – GPA: 3.83/4.0 Sep 2021 – Jun 2025
Relevant coursework: Digital Logic & Computer Organization, Computer System Programming, Artificial Intelligence, Natural Language Processing, Digital Signal and Image Processing

PUBLICATIONS

[1] ECG-LDC: Hardware-Efficient Low-Dimensional Computing Framework for ECG Arrhythmia Classification. **Anh Tran**, Khanh Tran, Cuong Do. *Under review*, 2026.

[2] Benchmarking and Charaterizing Timing Attack and Mitigation for RSA on Microcontrollers. **Anh Tran**. *Under review*, 2026.

EXPERIENCE

Research Assistant | VinUni–Illinois Smart Health Center | VinUniversity Jul 2025 – Present
Supervised by: Assistant Prof. Danh Cuong Do

- Led the ECG-LDC project, designing an ultra-lightweight Low-Dimensional Computing (LDC) model for ECG arrhythmia classification targeting edge wearable devices.
- Developed a hardware accelerator for ECG-LDC, leveraging compact binary representation and XOR-based computation.
- The model achieved competitive classification performance vs. SOTA with significant reductions in memory footprint, resource utilization, and power consumption. Resulting work is in preparation for publication.
- Currently working on advanced hardware synthesis of LDC for improved latency and resource efficiency.

Research Assistant | EDABK Research Lab | Hanoi University of Science and Technology Jun 2025 – Dec 2025
Supervised by: Assoc. Prof. Duc Minh Nguyen

- Developed a full deployment pipeline for deep neural networks on a MicroBlaze-centered System-on-Chip (SoC), targeting the Xilinx ZCU104 platform.
- Built a code generator to automatically produce HLS kernels for convolutional and fully connected layers from Pytorch, supporting both full-precision and quantized inference.
- Wrote driver code integrating HLS kernels with the MicroBlaze processor, with full support for DDR4, UART, and GPIO.

Research Assistant | Laurent's Group | VinUniversity May 2024 – Oct 2024
Supervised by: Prof. Laurent El Ghaoui

- Conducted research on implicit deep learning, an emerging paradigm proposed by Prof. Laurent El Ghaoui.
- Designed experiments to evaluate the generalization, sparsity, and representational capacity of implicit models across multiple architectures, including fully connected, residual, attention-based, and recurrent networks.
- Implemented and benchmarked fixed-point equation solvers (MOSEK, ADMM, and projected gradient descent), a key component in implicit model training.

Research Assistant | Center for Environmental Intelligence | VinUniversity Mar 2024 – Oct 2024
Supervised by: Assoc. Prof. Nidal Kamel

- Worked on developing a deep generative model for satellite image super-resolution, incorporating dynamic high-pass filtering and channel attention mechanisms to enhance image quality.
- Built a data preprocessing pipeline covering data cleaning, augmentation, and normalization for satellite imagery from Vietnam's mountainous and fores:t regions.
- Integrated super-resolved images as input to carbon stock estimator, using neural networks to refine prediction accuracy.

AI/Data Engineer Intern | AlphaAsimov Robotics Mar 2024 – Oct 2024

- Performed data preprocessing and analysis to ensure readiness for AI model training; assessed the alignment of various modalities (camera, LIDAR, SONAR, IMU, GPS, etc.) in the dataset.

- Designed tools using Python and Bash scripting, to streamline and partially automate the data verification process, incorporating anomaly detection models and descriptive visualizations.

TEACHING

CIS 5710: Computer Organization & Design | University of Pennsylvania Spring 2026
- Responsibilities included answering students' online questions, holding office hours, and grading/proctoring exams

ESE 5060: Introduction to Optimization Theory | University of Pennsylvania Fall 2025
- Responsibilities included answering students' online questions, grading homework, and grading/proctoring exams

PROJECTS

High-Performance CUDA Kernel for CSR-Dense Matrix Multiplication Oct 2025 – Mar 2026
- Designed a custom Compressed Sparse Row (CSR) $\times$ dense CUDA kernel with an optimized thread layout for coalesced access and minimized bank conflicts, along with shared-memory tiling to improve data reuse.
- Achieved up to $1.5\times$ speedup over cuSPARSE and $1.39\times$ speedup over torch.sparse baseline.
- Ongoing effort to explore additional optimization strategies, including load-balancing schemes across warps/threads and alternative work partitioning to further accelerate the kernel.

System-on-Chip (SoC) Design for Real-Time Data Deduplication and Compression Oct 2025 – Dec 2025
- Designed a comprehensive deduplication-compression pipeline integrating content-defined chunking (CDC), SHA-256 hashing, and LZW (Lempel-Ziv-Welch) compression.
- Enhanced hashing throughput using ARM NEON SIMD intrinsics and developed a FPGA-based accelerator for LZW.
- Demonstrated a performance exceeding 800 Mbps throughput with a 0.65 compression ratio on the Ultra96-V2 platform.

Pipelined RISC-V Processor Jan 2024 – May 2025
- Developed a custom 32-bit RISC-V core using SystemVerilog with a fully pipelined datapath, incorporating multicycle operators, direct-mapped instruction and data caches, and AXI4-Lite protocol for streamlined memory communication.
- Synthesized using the Yosys toolchain and deployed on Lattice ECP5 FPGA, achieving a 31 MHz maximum clock frequency with resource utilization of 30.9% LUTs and 4.1% flip-flops.

Fast, Compact and Efficient DNN via Pruning and Sparse Matrix Compression Oct 2024 – Dec 2024
- Explored various pruning strategies (global, channel-wise, hard pruning), combined with quantization, to reduce model size while maintaining accuracy and accelerating inference.
- Developed custom sparse linear layer leveraging Compressed Sparse Row (CSR) format for efficient storage and inference.
- Achieved a $1.52\times$ speedup in the most pruned layer and reduced the model size by 43% on VGG16 architecture.

Configurable Logic Block (CLB) Design and Optimization Oct 2024 – Dec 2024
- Designed a transistor-level 16-bit CLB circuit using 45nm Salicide CMOS technology in the Cadence toolchain.
- Performed transistor sizing, mitigated timing hazards, and optimized the circuit for minimal delay and energy efficiency.
- Achieved a maximum operating frequency of 1 GHz and an average power consumption of 134.9 W.

AWARDS & HONORS

Vingroup Science & Technology Scholarship, Full funding for Master's studies at Upenn 2024
Excel Award for Exceptional Capability, VinUniversity 2023
Dean's List for Excellent Academic Performance, VinUniversity 2021–2024
Undergraduate Merit-based Full-Tuition Scholarship, VinUniversity 2021
Gold Medal, Vietnamese National Physics Olympiad 2020
Gold Medal, Physics Competition for Specialized Students in the Northern Delta and Coastal Areas, Vietnam 2019

SKILLS & INTERESTS

Programming: C/C++, Python, Verilog, Assembly (ARM, RISC-V, x86), CUDA, MATLAB
Hardware Platforms: Avnet Ultra96-V2, Xilinx PYNQ-Z2, Xilinx ZCU104, ULX3S
Hardware Design & EDA Tools: Vitis HLS, Vivado Design Suite, Cadence Toolchain
Software & Systems Tools: Linux, Git, Docker, CUDA Toolkit
ML & Computing Frameworks: PyTorch, TensorFlow, TensorRT, JAX, OpenCV, OpenCL
Research Focus: ML Systems, Reconfigurable Computing, GPU Computing, Computer Architecture

OUTREACH & SERVICE

Speaker | Future Fest Day 7 – Global Live Talks 2026

- Delivered a talk at an event with 1500+ students on navigating university, research, and career preparation in the age of AI.

Co-Founder & Editor | Physiad – The Physics Magazine 2021 – 2023

- Co-founded a physics PopSci fanpage [link] with 18K+ followers targeting high school and early college students.
- Compiled and co-authored a problem set book covering electromagnetism topics for physics olympiad preparation: *Selected Problems in Electromagnetism from Physics Olympiads* [pdf] [code].